ABSTRACT

A PWM drive circuit of the present invention is built with a load driving power MOS transistor Q5 (Q6), a resistor R3 (R5) or R4 (R6), and a capacitance of the MOS transistor Q5 (Q6). The PWM drive circuit is provided with: a CR circuit that reduces a through rate of a voltage based on a PWM voltage and then feeds the resultant voltage to the gate of the MOS transistor Q5 (Q6); and a gate voltage control portion 4 (5) that stops an operation of the CR circuit and pulls down (up) the gate potential of the MOS transistor Q5 (Q6) to a predetermined value upon detecting during a transition period of a gate voltage of the MOS transistor Q5 (Q6) that the MOS transistor Q5 (Q6) is completely switched from off to on. This makes it possible to reduce switching noise and switching loss.